EXHIBIT 4

[redacted]

UNITED STATES DISTRICT COURT
EASTERN DISTRICT OF TEXAS
MARSHALL DIVISION

NETLIST, INC, Plaintiff, v. MICRON TECHNOLOGY, INC., MICRON SEMICONDUCTOR PRODUCTS, INC., and MICRON TECHNOLOGY TEXAS LLC Defendants.	Civil Case No. 2:22-cv-00203-JRG-RSP **JURY TRIAL DEMANDED**

DEFENDANTS' P.R. 3-3 INVALIDITY CONTENTIONS

Pursuant to Docket Control Order (Dkt. No. 40) and Local Patent Rule 3-3, Defendants Micron Technology, Inc., Micron Semiconductor Products, Inc., and Micron Technology Texas LLC (collectively, "Micron" or "Defendants") hereby provide their Invalidity Contentions, which include the accompanying claim charts concerning U.S. Patent Nos. 10,860,506 ("the '506 patent"), 10,949,339 ("the '339 patent"), 11,016,918 ("the '918 patent"), 11,232,054 ("the '054 patent"), 9,318,160 ("the '160 patent"), and 8,787,060 ("the '060 patent") (collectively, the "Asserted Patents") to Plaintiff Netlist, Inc. ("Plaintiff" or "Netlist").

The citation of prior art herein and the accompanying exhibits are not intended to reflect Defendants' claim construction contentions, which will be disclosed in due course in accordance with the Docket Control Order and may instead reflect Plaintiff's apparent (and potentially erroneous) claim constructions based on its Infringement Contentions.

I. Introduction

As disclosed in its P.R. 3-1 Infringement Contentions served on Defendants, Plaintiff

asserts the following patents and claims:

Patent	Claims
U.S. Patent No. 10,860,506	**1**, 2, 3, 5, 11, 12, 13, **14**, 15, 16
U.S. Patent No. 10,949,339	**1**, 2, 3, 4, 6, 7, 8, 9, 10, **11**, 12, 13, 14, 15, 16, 17, 18, **19**, 20, 21, 22, 23, 26, **27**, 28, 29, 30, 32, 33, 34, 35
U.S. Patent No. 11,016,918	**1**, 2, 3, 5, 6, 7, 9, 10, 11, 12, 13, 15, **16**, 17, 18, 19, 20, 21, 22, **23**, 24, 25, 26, 27, 28, 29, 30
U.S. Patent No. 11,232,054	**1**, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 15, **16**, 17, 23, **24**, 25, 29, 30
U.S. Patent No. 9,318,160	**1**, 2, 3, 4, 5, 6, 7, 8, 9, 10, **11**, 12, 13, 14, 16, 17, 18, 19, **20**, 21, 23, 24, 25, 26, 27, 28
U.S. Patent No. 8,787,060	**1**, 2, 4, 5

The claims identified above are referenced to as "the Asserted Claims" unless reference is made specifically with respect to particularly identified one or more of the Asserted Patents and/or one or more of the Asserted Claims.

As further detailed in and supported by these Invalidity Contentions, Defendants contend that each of the Asserted Claims is invalid under at least 35 U.S.C. §§ 101, 102, 103, and 112.[1] Defendants reserve the right to prove the invalidity of the Asserted Claims on bases other than those required to be disclosed in these disclosures pursuant to P.R. 3-3.

II. Amendment / Supplementation

Defendants' Invalidity Contentions pertain to the Asserted Claims as identified in Plaintiff's Infringement Contentions. To the extent the Court later allows Plaintiff to amend its infringement contentions and/or assert one or more claims other than the Asserted Claims, Defendants reserve the right to modify, amend, or supplement these Invalidity Contentions accordingly to, for example, show the invalidity of any such newly Asserted Claims.

[1] References to Title 35 of the United States Code are to statutes prior to amendments under the America Invents Act ("AIA").

These Invalidity Contentions are based on Defendants' current understanding of the Asserted Claims and Plaintiff's apparent view of the scope of those claims as shown, for example, in Plaintiff's Infringement Contentions. A *Markman* Order in this case has not yet been issued, and in no way shall these Invalidity Contentions be taken as any admission or acquiescence by Defendants as to the proper scope of the Asserted Claims and/or proper claim constructions of terms and phrases recited in those claims. By identifying prior art that anticipates and/or renders obvious the Asserted Claims, Defendants do not admit that the claim limitations are capable of construction, do not admit that any claim limitations are supported with an appropriate written description and enabling disclosure in the applicable patent specifications, and do not adopt Plaintiff's apparent claim constructions or admit the accuracy of any particular claim construction.[2] Defendants reserve all rights to later challenge or oppose any claim constructions advanced by Plaintiff and to present their own claim construction positions.

Defendants further reserve the right to revise these Invalidity Contentions in view of the Court's construction of terms and phrases recited in one or more of the Asserted Claims, additional information obtained during discovery, additional infringement theories put forth by Plaintiff during fact and/or expert discovery, any findings as to the priority date(s) of the Asserted Claims, and/or positions that Plaintiff, its fact witnesses, or its expert witness(es) may take concerning claim construction, infringement, and/or invalidity issues.

Defendants further reserve the right to supplement their accompanying P.R. 3-4(b)

[2] Defendants do not concede that Plaintiff's apparent interpretation of the claims is correct, but rather assert the well-established principle that whatever infringes a claim if later in time anticipates if earlier in time. *Bristol-Myers Squibb Co. v. Ben Venue Labs., Inc.*, 246 F.3d 1368, 1378 (Fed. Cir. 2001). Thus, where Plaintiff for purposes of its infringement case alleges that a feature of an accused product meets a particular limitation recited in one or more of the Asserted Claims, then that feature, should it be found in the prior art, would also cause that limitation to be met for invalidity purposes.

document production should they later discover additional prior art documents, information, testimony, prior art systems and related documentation, and/or software or hardware code, including information provided by third parties after the date of service of these Invalidity Contentions.

Defendants may further rely on inventor admissions concerning the scope or state of the prior art relevant to the Asserted Claims, the patent prosecution histories of the Asserted Patents, related patents and/or patent applications, any deposition or trial testimony of the named inventors on the Asserted Patents, and the papers filed and any evidence produced or submitted by Plaintiff in connection with these cases or other related litigation. Defendants reserve the right to contend that one or more of the Asserted Claims are invalid under 35 U.S.C. § 102(f) in the event Defendants obtain evidence that one or more of the named inventors did not invent the subject matter in the Asserted Claims.

Prior art not included in these Invalidity Contentions, whether known or not known to Defendants, may become relevant. In particular, Defendants are currently unaware of the extent, if any, to which Plaintiff will contend that limitations of the Asserted Claims are not disclosed in the prior art identified in these Invalidity Contentions. Accordingly, Defendants reserve the right to identify other references that would disclose the allegedly missing limitation(s) of the claimed method, device, or system.

The references identified in these Invalidity Contentions, which include the attached claim charts, may disclose the elements of the Asserted Claims explicitly and/or inherently, and/or they may be relied upon to show the state of the art in the relevant time frame.

References identified in these Invalidity Contentions, as well as the "References Cited" on the face of the Asserted Patents and the patents cited within the body of the Asserted Patents,

may be used to illustrate, but not limit the scope of, the state of the art to which the Asserted Patents pertain (i.e., at a time prior to the date of alleged inventions of the Asserted Claims of the Asserted Patents). Moreover, Defendants reserve the ability to rely on later identified sources of information, including but not limited to witness testimony and other discovery, to establish the state of the art in the relevant time frame pertaining to the Asserted Patents.

Because discovery has just recently begun, Defendants anticipate that additional prior art and invalidity bases may be found. Defendants' investigation and analysis of the prior art is continuing, and thus Defendants reserve the right to supplement, amend, and/or revise the information provided herein as Defendants conduct further investigation and/or analysis, including identifying, charting, and relying on additional references.

Additionally, in view of likely third-party discovery that will be taken, Defendants reserve the right to present additional items of prior art under 35 U.S.C. §§ 102(a), (b), (e), and/or (g) and/or § 103 located during discovery or further investigation, and to assert contentions of invalidity under 35 U.S.C. §§ 102(c), (d), or (f). For example, Defendants expect to issue subpoenas to third parties believed to have knowledge, documents, and/or other evidence concerning invalidity of one or more of the Asserted Claims.

In addition to the positions and prior art identified in these Invalidity Contentions (including the accompanying invalidity claim charts), Defendants also incorporate by reference all invalidity contentions, prior art,[3] and invalidity claim charts (including, without limitation, all anticipation positions, obviousness positions (including all prior art combinations and motivations to combine), indefiniteness positions, written description positions, and non-enablement positions) concerning one or more of the Asserted Patents, as disclosed at any time.

[3] Prior art appearing in the file histories of the Asserted Patents is not required to be separately produced by Defendants under P.R. 3-4(b).

This includes without limitation disclosures in previous or related litigation, in United States Patent & Trademark Office ("USPTO") proceedings, by the Plaintiff, or by the named inventors or any individuals associated with the prosecution and/or post-grant review of the Asserted Patents.

Specifically, for example, Defendants identify, as prior art upon which they may rely to show the invalidity of the Asserted Claims, the prior art references disclosed by parties in any other litigation involving one or more of the Asserted Patents, any patent related to any of the Asserted Patents, and/or any other patent allegedly assigned to Netlist claiming priority to the Asserted Patents (collectively, "Other Netlist Proceedings").

Plaintiff has a duty to produce to Defendants all relevant documents from the Other Netlist Proceedings including but not limited to all prior art, invalidity contentions, and expert reports on invalidity (among other relevant items).

Defendants reserve the right to supplement or otherwise amend these Invalidity Contentions in response to any relevant discovery provided by third parties, Plaintiff, opening or rebuttal expert reports, fact or expert depositions, or in response to any claim construction ruling(s) issued by this Court (regardless of how and when such ruling is made). Defendants also reserve the right to supplement or otherwise amend these Invalidity Contentions in response to any rebuttal evidence disclosed by Plaintiff or as otherwise may be necessary or appropriate under the circumstances.

III. P.R. 3-3(a) – Identification of Prior Art

Pursuant to P.R. 3-3(a), and subject to Defendants' reservation of rights, Defendants identify each item of prior art that anticipates or renders obvious the Asserted Claims below.[4] In

[4] Defendants' disclosure of prior art is premised on the alleged priority dates of the Asserted

addition to the prior art identified below and in the attached exhibits, Defendants incorporate by reference all prior art, exhibits, and detailed explanation in the petitions of how the Asserted Claims are obvious or anticipated by prior artas described in at least the following *inter partes* review proceedings pending before the United States Patent and Trademark Office: IPR2022-00639, IPR2022-00711, IPR2022-00999, IPR2022-00996, IPR2022-01428, IPR2022-01427, IPR2023-00203, IPR2023-00204, and IPR2023-00205.

A. U.S. Patent No. 10,860,506

Invalidity claim charts identifying disclosures in the references identified in Tables 1-A, 2-A, 3-A, and 4-A as to the Asserted Claims of the '506 patent are provided in attached Exhibits A1 through A23.

Table 1-A: Prior Art Patents and Printed Publications for the '506 patent

Ex.	Patent No. or Title (Primary Inventor/Author)	Date of Issue/ Publication	Filing Date
RA-1	Asserted Patent's Admitted Prior Art (APA)		
RA-2	U.S. Patent App. Pub. No. 2010/0312956 (Hirashi)	Dec. 9, 2010	June 3, 2010
RA-3	U.S. Patent App. Pub. No. 2007/0008791 (Butt)	Jan. 11, 2007	July 7, 2005
RA-4	U.S. Patent No. 8,020,022 (Tokuhiro)	Sept. 13, 2011	Sept. 12, 2008
RA-5	U.S. Patent App. Pub. No. 2006/0277355 (Ellsberry)	Dec. 7, 2006	June 1, 2005
RA-6	U.S. Patent No. 7,024,518 (Halbert)	April 4, 2006	Mar. 13, 2002

Patents as identified in Plaintiff's infringement contentions. Defendants contend Plaintiff is not entitled to the alleged priority dates and reserve the right to modify, amend, or supplement their invalidity contentions with additional prior art references if any Asserted Claim is shown to not be entitled to the respective alleged priority date or if Plaintiff alleges any other priority date for any of the Asserted Claims. Notwithstanding that reservation of rights, Defendants also reserve the right to argue that they have been unduly prejudiced should Plaintiff allege a different priority date for any of the Asserted Claims, and that accordingly Plaintiff should not be allowed to do so.

Ex.	Patent No. or Title (Primary Inventor/Author)	Date of Issue/ Publication	Filing Date
RA-7	U.S. Patent No. 7,289,386 (Bhakta)	Oct. 30, 2007	July 1, 2005
RA-8	U.S. Patent No. 8,391,089 (Chen)	March 5, 2013	Mar. 5, 2010
RA-9	U.S. Patent No. 8,111,565 (Kuroki)	Feb. 7, 2012	Sept. 29, 2009
RA-10	JEDEC FBDIMM Standards	March 2007	
RA-11	JEDEC SDRAM/DIMM Standards	January 2022, November 2008	
RA-12	U.S. Patent No. 8,001,434 (Lee)	Aug. 16, 2011	Apr. 13, 2009
RA-30	Shabana Aqueel & Kavita Khare, "A High Performance DDR3 SDRAM Controller," Vol. 1, Issue 1, International Journal of Electronics and Electrical Engineering (Aqueel)	July 2012	
RA-31	Young-Chan Jang, "A Self-Calibrating Per-Pin Phase Adjuster for Source Synchronous Double Data Rate Signaling in Parallel Interface," Vol. E94-A, No. 2, IEICE Trans. Fundamentals (Jang)	February 2011	
RA-32	Jang-Woo Lee et al., "Inter-Pin Skew Compensation Scheme for 3.2-Gb/s/pin Parallel Interface," Vol. 10, No. 1, Journal of Semiconductor Technology and Science (Jang-Woo Lee)	March 2010	
RA-33	A. Alexandropoulos et al., "A novel 1.8 V, 1066 Mbps, DDR2, DFI-compatible, Memory Interface," 2010 IEEE Annual Symposium on VLSI, 387 (Alexandropoulos)	2010	
RA-34	Moon-Sang Hwang et al., "27.3: 1.2 Gbps GDDR3 Physical Layer for 3D AMOLED Panel," SID 11 DIGEST (Hwang)	2011	
RA-35	U.S. Patent No. 7,562,271 (Shaeffer)	July 14, 2009	Apr. 6, 2007
RA-36	U.S. Patent No. 9,361,955 (Muralimanohar)		Jan. 27, 2011/ Jan. 28, 2010 (prov)
RA-37	U.S. Patent No. 8,806,116 (Karamcheti)	Aug. 20, 2009	Feb. 11, 2009/ Feb. 12, 2008 (prov)
RA-38	U.S. Patent no. 7,181,584 (LaBerge)	Feb. 20, 2007	Feb. 5, 2004
RA-39	U.S. Patent no. 7,861,043 (Uchida)	Dec. 28, 2010	Feb. 9, 2006

Ex.	Patent No. or Title (Primary Inventor/Author)	Date of Issue/ Publication	Filing Date
RA-40	U.S. Patent no. 9,195,602 (Hampel)	May 6, 2010	Mar. 19, 2008/ Mar. 30, 2007 (prov.)

Table 2-A: Prior Art Systems and Inventions for the '506 patent

Ex.	Name of System or Invention	Date of Sale / Offer for Sale / Public Use
RA-13	SK hynix 178ball FBGA System (SK Hynix FBGA)	At least as early as July 2012
RA-14	Elpida DDR3 SDRAM System (Elpida DDR3 SDRAM)	At least as early as March 2009
RA-15	JEDEC Proposals and Minutes regarding FBDIMM (JEDEC FBDIMM Proposals)	At least as early as October 2004, May 2006, June 2006, August 2007, March 2008
RA-16	JEDEC Proposals and Minutes regarding SDRAM/DIMM (JEDEC SDRAM/DIMM Proposals)	At least as early as November 2010, March 2011, June 2011, August 2011, September 2011, March 2012
RA-17	Lattice Semiconductor DDR3 System (Lattice DDR3)	At least as early as March 2010
RA-18	NXP DDR System (NXP DDR)	At least as early as June 2010
RA-19	Kentron's Quad Band Memory System (QBM)	At least as early as 1999-2005
RA-20	SDRAM Controller for the MORPHEUS Reconfigurable Architecture (MORPHEUS SDRAM Controller)	At least as early as April 2008
RA-21	Altera External Memory Interface System, as described in "ALTDLL and ALTDQ_DQS Megafunctions User Guide" (Altera 1)	At least as early as February 2012
RA-22	Altera External Memory Interface System, as described in "External Memory Interface Handbook, Volume 4: Simulation, Timing Analysis, and Debugging" (Altera 2)	At least as early as June 2011
RA-23	Altera External Memory Interface System, as described	At least as early as March

Ex.	Name of System or Invention	Date of Sale / Offer for Sale / Public Use
	in "External Memory Interfaces in HardCopy IV Devices" (Altera 3)	2012
RA-24	Altera External Memory Interface System, as described in "Challenges in Implementing DDR3 Memory Interface on PCB Systems - A Methodology for Interfacing DDR3 SDRAM DIMM to an FPGA" (Altera 4)	At least as early as 2008
RA-25	DFi DDR PHY Interface System, as described in "DDR PHY Interface (DFI) Specification" (DFi DDR PHY 1)	At least as early as January 2009
RA-26	DFi DDR PHY Interface System, as described in "DFI 3.0 Specification" (DFi DDR PHY 2)	At least as early as May 2012
RA-27	NXP MSC8152 System, as described in "MSC8152 Reference Manual" (NXP MSC8152)	At least as early as June 2011
RA-28	Xilinx Processing System, as described in "Zynq-7000 Extensible Processing Platform: Technical Reference Manual" (Xilinx 1)	At least as early as May 2012
RA-29	Xilinx Processing System, "Implementing High-Performance Interfaces with Virtex-4 FPGAs" (Xilinx 2)	At least as early as January 2006

Defendants have obtained or are in the process of obtaining the identified devices and will make them available for inspection. To the extent that one or more documents (*e.g.*, user manual) may be used to describe aspects of a particular device, that device is a single reference for prior art purposes under 35 U.S.C. § 102. Some or all of the corroborating references may also separately qualify as prior art publications under 35 U.S.C. § 102 and may be used as invalidating references under 35 U.S.C. §§ 102 and/or 103.

Further, Defendants are actively searching for information regarding at least the following devices and inventions:

- SK hynix America Inc.'s 178ball FBGA System
- Micron Technology, Inc.'s Elpida DDR3 SDRAM System

- Lattice Semiconductor Corp.'s DDR3 System
- NXP Semiconductors's Freescale Semiconductor DDR System
- Kentron's Quad Band Memory System
- Institut für Technik der Informationsverarbeitung (ITIV), University of Karlsruhe's SDRAM Controller for the MORPHEUS Reconfigurable Architecture

Discovery is ongoing, and Defendants may serve other third parties with document subpoenas. One or more of these devices, along with related documentation, may be invalidating, and Defendants reserve the right to supplement these contentions accordingly.

In addition, Defendants identify, responsive to Plaintiff's infringement contentions, the following patents, publications, and systems as evidence of the state of the art as it relates to memory modules:

- U.S. Patent App. Pub. No. 2010/0312956 (Hirashi) at Fig. 1, [0010], and [0011].
- U.S. Patent App. Pub. No. 2007/0008791 (Butt) at Fig. 1, Fig. 2, [0003], [0005], [0015], and [0017].
- U.S. Patent No. 8,020,022 (Tokuhiro) at Fig. 4, 3:16-43, and 4:62-5:30.
- U.S. Patent App. Pub. No. 2006/0277355 (Ellsberry) at Fig. 2, [0002], [0010], [0011], and [0012].
- U.S. Patent No. 7,024,518 (Halbert) at Fig. 4., 3:42-4:8, and 4:36-5:65.
- U.S. Patent No. 7,289,386 (Bhakta) at Fig.1, Fig. 2, Fig. 3, and 2:46-3:30.
- U.S. Patent No. 8,391,089 (Chen) at Fig. 4, 1:22-2:6, 4:3-30, and 5:4-52.
- U.S. Patent No. 8,111,565 (Kuroki) at Fig. 4B, 1:4-33, and 2:52-3:48.
- SK Hynix 178ball FBGA System at page 11 and page 128.
- Elpida DDR3 SDRAM System at page 12, page 13, and page 15.

- Lattice Semiconductor DDR3 System at Fig. 1, Fig. 2, page 2, and page 4.
- NXP DDR System at page 33, page 35, and page 36.
- Kentron Technologies Inc.'s Quad Band Memory System, QBM Specification Rev. 0.93 at page 6 and page 9.
- SDRAM Controller for the MORPHEUS Reconfigurable Architecture at Fig. 1, Fig. 3, page 1, and page 5.
- U.S. Patent No. 7,562,271 B2 (Shaeffer) at Fig. 5, 3:26–39, 4:18–42, 5:11–20, 9:29–51.
- U.S. Patent No. 9,361,955 (Muralimanohar) at Figs. 1, 2, 4, 9, 4:6–67, 5:1–58, 6:25–53, 7:5–8:25, 24:23–44.
- U.S. Patent No. 8,806,116 (Karamcheti) at Figs. 1–6, 13, and accompanying disclosures, 1:8–32, 2:40–3:48, 8:63–9:26, 18:1–13.

Each of these references show that the concept of implementing delays in memory modules is not novel and was well-known for many years. In light of the references discussed herein, the Asserted Claims of the '506 patent cannot be valid.

Defendants continue to investigate each of the identified devices, including through potential discovery needed to be obtained via third party subpoenas, and reserve the right to supplement these contentions and accompanying claim charts after further investigation.

Defendants' reference to a particular product, device, or software program in these contentions should be interpreted as a reference to the system itself and any corresponding patents, publications, or product literature relating to the cited system. Upon information and belief, the systems were publicly disclosed, used, sold, or offered for sale in the United States before the alleged priority date of the Asserted Claims of the '506 patent. Defendants'

investigation of such prior art systems is still ongoing and discovery has not yet been received from third parties who may have information concerning such prior art systems. Accordingly, subsequent discovery may reveal information that affects the disclosures and contentions herein. For example, subsequent discovery may provide additional information regarding whether or not any of the third party prior art systems anticipate or render obvious the Asserted Claims of the '506 patent. As such, Defendants reserve all rights to supplement their invalidity contentions.

Many of the inventive, research, design, and development activities concerning these systems and technologies occurred in the United States before the alleged priority date of the Asserted Claims of the '506 patent. Defendants are in the process of obtaining additional information regarding the dates by which the cited products and services were publicly disclosed, used, sold, or offered for sale, the circumstances under which the research, design, and development activities were conducted, and the identities of the particular individuals involved in such activities through publicly available patents, publications, and product literature. The actual dates, circumstances, and identities of individuals will be the subject of third party discovery during this lawsuit, which Defendants reserve the right to rely upon to corroborate the prior art status of the prior art identified herein. Defendants reserve the right to modify, amend, or supplement these contentions if additional information becomes available during the course of this lawsuit. Furthermore, Defendants will make all such devices, software programs, or other products in Defendants' possession, custody, or control available for inspection by Plaintiff.

Consequently, Defendants reserve the right to amend, modify, or supplement these Invalidity Contentions should additional information become available to them through discovery.

Table 3-A provides additional bases for invalidity of the '506 patent under pre-AIA 35

U.S.C. § 102(f), on the grounds that the inventors of the '506 patent did not themselves invent the subject matter claimed in the '506 patent. The prior art under § 102(f) is identified in Table 3 by the name of the person(s) from whom the invention was derived. The circumstances under which the invention was derived are explained below.

Table 3-A: Prior Art under pre-AIA § 102(f) for the '506 patent

Ex.	Prior Art Disclosing Technical Features	Name of Person(s) from Whom Invention was Derived
RA-19	Quad Band Memory (QBM) System ("*QBM*")	Kentron Technologies Inc. employee(s) (*e.g.*, Chris Karabatsos, Vasilios Karabatsos, Bob Goodman, Badawi Dweik)
RA-15	Proposals and disclosures made at JEDEC committee meetings during the time period 2004-2008 ("*JEDEC FBDIMM Proposals*")	Entities and persons attending JEDEC committee meetings where related technology was discussed (including the JC-40 and JC-45 committee meetings). For example: • One or more employees of Intel Corp. • One or more employees of Qimonda • One or more employees of Nanya Technology Corporation • One or more employees of Staktek Corporation
RA-16	Proposals and disclosures made at JEDEC committee meetings during the time period 2010-2012 ("*JEDEC SDRAM/DIMM Proposals*")	Entities and persons attending JEDEC committee meetings where related technology was discussed (including the JC-40 and JC-45 committee meetings). For example: • One or more employees of Intel Corp. • One or more employees of Elpida Memory, Inc. • One or more employees of Inphi Corporation

QBM

Between at least 1999 and 2005, Kentron Technologies Inc. ("Kentron") invented and

developed memory modules based on its Quad Band Memory (*QBM*) technology, well before the July 27, 2012 alleged priority date of the '506 patent. During this time period, Kentron formed the QBM Alliance, an alliance of technology partners aimed at positioning QBM as an industry standard. *See, e.g.*, SAM-NET00315873.[5] The technical details of the QBM system were regularly disclosed to QBM Alliance members during this time period. *See, e.g.*, SAM-NET00315870-900, SAM-NET00315912. Netlist became a QBM Alliance member in February 2002. *See, e.g.*, SAM-NET00315845-47; SAM-NET00315874-81. Because Netlist was a QBM Alliance member, Micron has reason to believe that Netlist knew about the technical features of the QBM system and derived the claimed subject matter of the '506 patent from the QBM features. The technical features of QBM are shown in the following documents: SAM-NET00314833 - SAM-NET00315913. The invalidity claim chart identifying disclosures from these documents as to the Asserted Claims of the '506 patent is provided in attached Exhibit A18.

JEDEC Proposals

Hyun Lee – an inventor of the '506 patent – regularly attended JEDEC meetings for at least the JC-40 committee and the JC-45 committee in 2011 and 2012, as well as before and after that timeframe, and before the alleged July 27, 2012 priority date of the '506 patent.

By virtue of his attendance at those meetings, active involvement in JEDEC and otherwise, Micron has reason to believe that Hyun Lee was aware of the draft and final specifications for DDR4 LRDIMMs being considered and voted upon by those committees,

[5] Defendants, via subpoena, obtained the infringement contentions and prior art used in Samsung's invalidity contentions against the same Asserted Claims involved *in Netlist, Inc. v. Samsung Electronics Co., Ltd. et al.*, 2:21-cv-00463-JRG (E.D. Tex.). These contentions refer to the Bates number for documents that Samsung has already produced to Netlist in that case.

including JESD82-32, dated November 2016, as well as prior drafts of it. For example, Intel presented and discussed Committee Item Number 158.01 ("DDR4 LRDIMM Proposal") at the December 8, 2011 meeting of JC-40, Committee Item Number 0311.14 ("Proposed DDR4 DB Training Modes") at the March 25, 2012 meeting of JC-40, and Committee Item Number 0311.12 ("Proposed DDR DB Buffer Control Words") at the June 4, 2012 meeting of JC-40, all of which Hyun Lee attended.

Draft specifications, ballots and presentations distributed to the members of the JC-40 and/or JC-45 committees of JEDEC were distributed to many (20+) key members of the interested public with the expectation they would be freely disclosed to and discussed with others. Based on Netlist's apparent view of the scope of the alleged invention, each of the draft DDR4 LRDIMM drafts and presentations disclose materially the same structure and functionality that Netlist accuses of infringing the claims of '506 patent.

After attending the June 4, 2012 meeting and listening to these ideas from other members of JEDEC, Hyun Lee returned to Netlist and drafted the provisional application to which the '506 patent claims priority, and which Micron has reason to believe contained a significant amount of material Hyun Lee and Netlist learned at JEDEC. Hyun Lee filed the provisional application on July 27, 2012, naming himself as the inventor.

Table 4 below provides additional bases for invalidity of the '506 patent under pre-AIA 35 U.S.C. § 102(g)(2), on the grounds that the alleged invention of the '506 patent was made in this country before the alleged invention date of the '506 patent by another inventor who had not abandoned, suppressed, or concealed it. The prior art under § 102(g)(2) is identified in Table 4 by the name of the person(s) or entities involved in the making of the invention before the applicants of the '506 patent. The circumstances surrounding the making of the invention before

the applicants of the '506 patent are explained below.

Table 4-A: Prior Art under pre-AIA § 102(g)(2) for the '506 patent

Ex.	Prior Art Disclosing Technical Features	Name of Person(s) from Whom Invention was Derived
RA-19	Quad Band Memory (QBM) System ("*QBM*")	Kentron Technologies Inc. employee(s) (*e.g.*, Chris Karabatsos, Vasilios Karabatsos, Bob Goodman, Badawi Dweik)
RA-15	Proposals and disclosures made at JEDEC committee meetings during the time period 2004-2008 ("*JEDEC FBDIMM Proposals*")	Entities and persons attending JEDEC committee meetings where related technology was discussed (including the JC-40 and JC-45 committee meetings). For example: • One or more employees of Intel Corp. • One or more employees of Qimonda • One or more employees of Nanya Technology Corporation • One or more employees of Staktek Corporation
RA-16	Proposals and disclosures made at JEDEC committee meetings during the time period 2010-2012 ("*JEDEC SDRAM/DIMM Proposals*")	Entities and persons attending JEDEC committee meetings where related technology was discussed (including the JC-40 and JC-45 committee meetings). For example: • One or more employees of Intel Corp. • One or more employees of Elpida Memory, Inc. • One or more employees of Inphi Corporation

QBM

Between at least 1999 and 2005, Kentron Technologies Inc. ("Kentron") invented and developed memory modules based on its Quad Band Memory (*QBM*) technology, well before the

July 27, 2012 alleged priority date of the '506 patent. During this time, Kentron formed the QBM Alliance, an alliance of technology partners aimed at positioning QBM as an industry standard. *See*, *e.g.*, SAM-NET00315873. The technical details of the QBM system were regularly disclosed to QBM Alliance members during this time period. *See, e.g.*, SAM-NET00315870-900, SAM-NET00315912. Netlist became a QBM Alliance member in February 2002. *See*, *e.g.*, SAM-NET00315845-47, SAM-NET00315874-81. Because Netlist was a QBM Alliance member, Micron has reason to believe that Netlist knew about the technical features of the QBM system and used the technical features of the QBM system to draft the provisional application to which the '506 patent claims priority as well as the claims of the '506 patent. The technical features of QBM are shown in the following documents: SAM-NET00314833 - SAM-NET00315913. The invalidity claim chart identifying disclosures from these documents as to the Asserted Claims of the '506 patent is provided in attached Exhibit A18. Kentron did not abandon, suppress, or conceal its invention of QBM. Kentron presented the technical features of QBM to JEDEC, described the features in newsletters to its QBM Alliance members, and filed patents covering the technology. *See, e.g.*, SAM-NET00313593-615, SAM-NET00315870- 900, SAM-NET00315171-87, SAM-NET00313434.

JEDEC Proposals

Hyun Lee – an inventor of the '506 patent – regularly attended JEDEC meetings for at least the JC-40 committee and the JC-45 committee in 2011 and 2012, as well as before and after that timeframe, and before the alleged July 27, 2012 priority date of the '506 patent.

By virtue of his attendance at those meetings, active involvement in JEDEC and otherwise, Hyun Lee was aware of the draft and final specifications for DDR4 LRDIMMs being considered and voted upon by those committees, including JESD82-32, dated November 2016,

as well as prior drafts of it. For example, Intel presented and discussed Committee Item Number 158.01 ("DDR4 LRDIMM Proposal") at the December 8, 2011 meeting of JC-40, Committee Item Number 0311.14 ("Proposed DDR4 DB Training Modes") at the March 25, 2012 meeting of JC-40, and Committee Item Number 0311.12 ("Proposed DDR DB Buffer Control Words") at the June 4, 2012 meeting of JC-40, all of which Hyun Lee attended.

Draft specifications, ballots and presentations distributed to the members of the JC-40 and/or JC-45 committees of JEDEC were distributed to many (20+) key members of the interested public with the expectation they would be freely disclosed to and discussed with others. Therefore, they were not abandoned, suppressed, or concealed. Based on Netlist's apparent view of the scope of the alleged invention, each of the draft DDR4 LRDIMM drafts and presentations disclose materially the same structure and functionality that Netlist accuses of infringing the claims of '506 patent.

After attending the June 4, 2012 meeting and listening to these ideas from other members of JEDEC, Hyun Lee returned to Netlist and drafted the provisional application to which the '506 patent claims priority, and which Micron has reason to believe contained a significant amount of material Hyun Lee and Netlist learned at JEDEC. Hyun Lee filed the provisional application on July 27, 2012, naming himself as the inventor.

With discovery ongoing, Defendants reserve the right to amend, modify, or supplement these Invalidity Contentions with additional 35 U.S.C. §102(f) and/or (g) allegations should additional information become available through discovery supporting such allegations.

B. U.S. Patent No. 10,949,339

Invalidity claim charts identifying disclosures in the references identified in Tables 1-B, 2-B, 3-B, and 4-B to the Asserted Claims of the '339 patent are provided in attached Exhibits B1 through B25.

Table 1-B: Prior Art Patents and Printed Publications for the '339 patent

Ex.	Patent No. or Title (Primary Inventor/Author)	Date of Issue/ Publication	Filing Date
RB-1	Asserted Patent's Admitted Prior Art (APA)		
RB-2	U.S. Patent App. Pub. No. 2006/0277355 (Ellsberry)	Dec. 7, 2006	June 1, 2005
RB-3	U.S. Patent No. 7,024,518 (Halbert)	April 4, 2006	Mar. 13, 2002
RB-4	U.S. Patent No. 7,532,537 (Solomon)	May 12, 2009	June 19, 2006
RB-5	U.S. Patent No. 6,530,033 (Raynham)	March 4, 2003	Oct. 28, 1999
RB-6	U.S. Patent No. 6,947,304 (Yen)	Sept. 20, 2005	May 12, 2003
RB-7	U.S. Patent App. Pub. No. 2008/0028135 (Rajan)	Jan. 31, 2008	Jan. 31, 2008
RB-8	U.S. Patent No. 6,972,981 (Ruckerbauer)	Dec. 6, 2005	July 30, 2004
RB-9	U.S. Patent No. 7,389,375 (Gower 375)	June 17, 2008	July 30, 2004
RB-10	U.S. Patent No. 7,512,762 (Gower 762)	March 31, 2009	Oct. 29, 2004
RB-11	U.S. Patent No. 7,395,476 (Cowell)	July 1, 2008	Oct. 29, 2004
RB-12	U.S. Patent No. 6,714,433 (Doblar)	March 30, 2004	June 15, 2001
RB-13	U.S. Patent No. 7,289,386 (Bhakta)	Oct. 30, 2007	Oct. 30, 2007
RB-14	JEDEC SDRAM/DIMM Standards	June 2000, January 2002, January 2004, January 2005, November 2008	
RB-15	JEDEC FBDIMM Standards	March 2007	

Ex.	Patent No. or Title (Primary Inventor/Author)	Date of Issue/ Publication	Filing Date
RB-16	U.S. Patent No. 8,001,434 (Lee)	Aug. 16, 2011	Apr. 13, 2009
RB-25	Hongzhong Zheng et al., "Mini-Rank: Adaptive DRAM Architecture for Improving Memory Power Efficiency," IEEE (Hongzhong Zheng)	2008	
RB-26	U.S. Patent App. Pub. No. 2009/0210616 (Karamcheti)	Aug. 20, 2009	Feb. 11, 2009
RB-27	U.S. Patent App. Pub. No. 2008/0080261 (Shaeffer)	Apr. 3, 2008	Apr. 6, 2007

Table 2-B: Prior Art Systems and Inventions for the '339 patent

Ex.	Name of System or Invention	Date of Sale / Offer for Sale / Public Use
RB-17	JEDEC Proposals and Minutes regarding SDRAM/DIMM (JEDEC SDRAM/DIMM Proposals)	At least as early as May 2008, December 2008, February 2009
RB-18	JEDEC Proposals and Minutes regarding FBDIMM (JEDEC FBDIMM Proposals)	At least as early as October 2004, May 2006, June 2006, August 2007, March 2008
RB-19	Micron DDR2 SDRAM FBDIMM	At least as early as December 2009
RB-20	IBM Z990 eServer	At least as early as May-July 2004
RB-21	Kentron's Quad Band Memory System (QBM)	At least as early as 1999-2005
RB-22	Samsung DDR3 SDRAM	At least as early as April 2009
RB-23	Samsung DDR2 FBDIMM	At least as early as January 2008
RB-24	Kingston Fully Buffered DIMM System, as described in "Fully Buffered DIMM FAQ" (Kingston FBDIMM)	At least as early as 2006

Defendants have obtained or are in the process of obtaining the identified devices and will make them available for inspection. To the extent that one or more documents (*e.g.*, user

manual) may be used to describe aspects of a particular device, that device is a single reference for prior art purposes under 35 U.S.C. § 102. Some or all of the corroborating references may also separately qualify as prior art publications under 35 U.S.C. § 102 and may be used as invalidating references under 35 U.S.C. §§ 102 and/or 103.

Further, Defendants are actively searching for information regarding at least the following devices and inventions:

- International Business Machines Corp. (IBM)'s Z990 eServer
- Kentron Technologies Inc.'s Quad Band Memory System (QBM)

Discovery is ongoing, and Defendants may serve third parties with document subpoenas.

One or more of these devices, along with related documentation, may be invalidating, and Defendants reserve the right to supplement these contentions accordingly.

In addition, Defendants identify, responsive to Plaintiff's infringement contentions, the following patents, publications, and systems as evidence of the state of the art as it relates to memory modules:

- U.S. Patent App. Pub. No. 2006/0277355 (Ellsberry) at Fig. 2, [0002], [0010], [0011], and [0012].
- U.S. Patent No. 7,024,518 (Halbert) at Fig. 4, 3:43-4:8, and 4:36-5:65.
- U.S. Patent No. 7,532,537 (Solomon) at Fig. 1, Fig. 9A, 2:62-3:34, and 4:56- 5:2.
- U.S. Patent No. 6,530,033 (Raynham) at Fig. 4A 5:37-6:24, and 7:33-8:11.
- U.S. Patent No. 6,947,304 (Yen) at Fig. 5, 3:22-42, and 4:37-64.
- U.S. Patent App. Pub. No. 2008/0028135 (Rajan) at Fig. 2B, Fig. 3, [0017], [0074], and [0075].
- U.S. Patent No. 6,972,981 (Ruckerbauer) at Fig. 2, 3:50-66, and 4:45-57.

- U.S. Patent No. 7,389,375 (Gower 375) at Fig. 10, Fig. 11, Fig 12, 2:40-3:13, and 5:38-58.
- U.S. Patent No. 7,512,762 (Gower 762) at Fig. 10, 2:59-3:26, and 5:41-6:22.
- U.S. Patent No. 7,395,476 (Cowell) at Fig. 10, Fig. 11, 3:3-38, and 6:21-54.
- U.S. Patent No. 6,714,433 (Doblar) at Fig. 2, 2:66-3:17, and 6:12-34.
- U.S. Patent No. 7,289,386 (Bhakta) at at Fig.1, Fig. 2, Fig. 3, and 2:46-3:30.
- Micron DDR2 SDRAM FBDIMM at Fig. 2, Fig. 3, Fig. 4, page 1, and page 7.
- IBM's Z990 eServer at Fig. 3, Fig. 4, Fig 11, page 370, and page 372.
- Kentron's Quad Band Memory System (QBM), QBM Specification Rev. 0.93 at page 6 and page 9.
- Samsung Electronics Co., Ltd.'s DDR3 SDRAM.
- Samsung Electronics Co., Ltd.'s DDR2 FBDIMM.
- Micron Technology, Inc.'s DDR2 FBDIMM.
- U.S. Patent App. Pub. No. 2008/0080261 at FIGS. 5-8, 9A-C, 10, 16, 17, 18, 27-30, 36-39 and related disclosures.
- U.S. Patent App. Pub. No. 2009/0210616 at FIGS. 1-5 and related disclosures.

Each of these references show that the concept of controlling the transmission of data signals is not novel. In light of the references discussed herein, the Asserted Claims of the '339 patent cannot be valid.

Defendants continue to investigate each of the identified devices, including through potential discovery needed to be obtained via third party subpoenas, and reserve the right to supplement these contentions and accompanying claim charts after further investigation.

Defendants' reference to a particular product, device, or software program in these

contentions should be interpreted as a reference to the system itself and any corresponding patents, publications, or product literature relating to the cited system. Upon information and belief, the systems were publicly disclosed, used, sold, or offered for sale in the United States before the alleged priority date of the Asserted Claims of the '339 patent. Defendants' investigation of such prior art systems is still ongoing and discovery has not yet been received from third parties who may have information concerning such prior art systems. Accordingly, subsequent discovery may reveal information that affects the disclosures and contentions herein. For example, subsequent discovery may provide additional information regarding whether or not any of the third party prior art systems anticipate or render obvious the Asserted Claims of the '339 patent. As such, Defendants reserve all rights to supplement their invalidity contentions.

Many of the inventive, research, design, and development activities concerning these systems and technologies occurred in the United States before the alleged priority date of the Asserted Claims of the '339 patent. Defendants are in the process of obtaining additional information regarding the dates by which the cited products and services were publicly disclosed, used, sold, or offered for sale, the circumstances under which the research, design, and development activities were conducted, and the identities of the particular individuals involved in such activities through publicly available patents, publications, and product literature. The actual dates, circumstances, and identities of individuals will be the subject of third party discovery during this lawsuit, which Defendants reserve the right to rely upon to corroborate the prior art status of the prior art identified herein. Defendants reserve the right to modify, amend, or supplement these contentions if additional information becomes available during the course of this lawsuit. Furthermore, Defendants will make all such devices, software programs, or other products in Defendants' possession, custody, or control available for inspection by Plaintiff.

Consequently, Defendants reserve the right to amend, modify, or supplement these Invalidity Contentions should additional information become available to them through discovery.

Table 3-A provides additional bases for invalidity of the '339 patent under pre-AIA 35 U.S.C. § 102(f), on the grounds that the inventors of the '339 patent did not themselves invent the subject matter claimed in the '339 patent. The prior art under § 102(f) is identified in Table 3 by the name of the person(s) from whom the invention was derived. The circumstances under which the invention was derived are explained below.

Table 3-B: Prior Art under pre-AIA § 102(f) for the '339 patent

Ex.	Prior Art Disclosing Technical Features	Name of Person(s) from Whom Invention was Derived
RB-21	Quad Band Memory (QBM) System ("*QBM*")	Kentron Technologies Inc. employee(s) (*e.g.*, Chris Karabatsos, Vasilios Karabatsos, Bob Goodman, Badawi Dweik)
RB-18	Proposals and disclosures made at JEDEC committee meetings during the time period 2004-2008 ("*JEDEC FBDIMM Proposals*")	Entities and persons attending JEDEC committee meetings where related technology was discussed (including the JC-40 and JC-45 committee meetings). For example: • One or more employees of Intel Corp. • One or more employees of Qimonda • One or more employees of Nanya Technology Corporation • One or more employees of Staktek Corporation
RB-17	Proposals and disclosures made at JEDEC committee meetings during the time period 2008-2009 ("JEDEC SDRAM/DIMM Proposals")	Entities and persons attending JEDEC committee meetings where related technology was discussed (including the JC-40 and JC-45 committee meetings). For example: • One or more employees of Intel Corp. • One or more employees of Elpida Memory, Inc.

Ex.	Prior Art Disclosing Technical Features	Name of Person(s) from Whom Invention was Derived
		• One or more employees of Inphi Corporation • One or more employees of Qimonda • One or more employees of FormFactor Inc.

QBM

Between at least 1999 and 2005, Kentron Technologies Inc. ("Kentron") invented and developed memory modules based on its Quad Band Memory (*QBM*) technology, well before the July 16, 2009 alleged priority date of the '339 patent. During this time period, Kentron formed the QBM Alliance, an alliance of technology partners aimed at positioning QBM as an industry standard. *See*, *e.g.*, SAM-NET00315873. The technical details of the QBM system were regularly disclosed to QBM Alliance members during this time period. *See, e.g.*, SAM-NET00315870-900, SAM-NET00315912. Netlist became a QBM Alliance member in February 2002. *See*, *e.g.*, SAM-NET00315845-47; SAM-NET00315874-81. Because Netlist was a QBM Alliance member, Micron has reason to believe that Netlist knew about the technical features of the QBM system and derived the claimed subject matter of the '339 patent from the QBM features. The technical features of QBM are shown in the following documents: SAM-NET00314833 - SAM-NET00315913. The invalidity claim chart identifying disclosures from these documents as to the Asserted Claims of the '339 patent is provided in attached Exhibit B20.

JEDEC Proposals

During the time period from at least 2005 to 2012, Netlist regularly attended JEDEC meetings for at least the JC-40 and JC-45 committees, including meetings that occurred before

the July 16, 2009 alleged priority date of the '339 patent. See, e.g., SAM-NET00005551-75; SAM-NET00008503-51; SAM-NET00008664-8700; SAM-NET00008847-67; SAM-NET00019805-18; SAM-NET00020197-98; SAM-NET00023999-24003; SAM-NET00026641-95; SAM-NET00026696-715; SAM-NET00040933-87; SAM-NET00040988-41007; SAM-NET00048535-608; SAM-NET00052084-131; SAM-NET00052132-50; SAM-NET00052917-20; SAM-NET00060465-532; SAM-NET00071314-88; SAM-NET00092148-53; SAM-NET00113524-54; SAM-NET00113555-67.

By virtue of Netlist's attendance at those meetings, active involvement in JEDEC and otherwise, Micron has reason to believe that Netlist was aware of the proposals and drafts being considered and voted upon by those committees. The proposals, drafts, ballots and presentations distributed to the members of the JEDEC committees were distributed to many (20+) key members of the interested public with the expectation they would be freely disclosed to and discussed with others. Based on Netlist's apparent view of the scope of the alleged invention, the proposals, drafts, and presentations disclose materially the same structure and functionality that Netlist accuses of infringing the claims of '339 patent.

After attending these meetings and listening to these ideas from other members of JEDEC, Netlist drafted the application to which the '339 patent claims priority, which Micron has reason to believe contained a significant amount of material Netlist learned at JEDEC.

Table 4 below provides additional bases for invalidity of the '339 patent under pre-AIA 35 U.S.C. § 102(g)(2), on the grounds that the alleged invention of the '339 patent was made in this country before the alleged invention date of the '339 patent by another inventor who had not abandoned, suppressed, or concealed it. The prior art under § 102(g)(2) is identified in Table 4 by the name of the person(s) or entities involved in the making of the invention before the

applicants of the '339 patent. The circumstances surrounding the making of the invention before the applicants of the '506 patent are explained below.

Table 4-B: Prior Art under pre-AIA § 102(g)(2) for the '339 patent

Ex.	Prior Art Disclosing Technical Features	Person(s)/Entity(ies) Involved
RB-21	Quad Band Memory (QBM) System ("QBM")	Kentron Technologies Inc. employee(s) (*e.g.*, Chris Karabatsos, Vasilios Karabatsos, Bob Goodman, Badawi Dweik)
RB-18	Proposals and disclosures made at JEDEC committee meetings during the time period 2004-2008 ("*JEDEC FBDIMM Proposals*")	Entities and persons attending JEDEC committee meetings where related technology was discussed (including the JC-45 committee meetings). For example: • One or more employees of Intel Corp. • One or more employees of Qimonda • One or more employees of Nanya Technology • One or more employees of Staktek Corp
RB-17	Proposals and disclosures made at JEDEC committee meetings during the time period 2008-2009 ("JEDEC SDRAM/DIMM Proposals")	Entities and persons attending JEDEC committee meetings where related technology was discussed (including the JC-40 and JC-45 committee meetings). For example: • One or more employees of Intel Corp. • One or more employees of Elpida Memory, Inc. • One or more employees of Inphi Corporation • One or more employees of Qimonda • One or more employees of FormFactor Inc.
RB-16	U.S. Patent No. 8,001,434 to Lee et al. (Lee), filed on Apr. 13, 2009, and issued on Aug. 16, 2011	Hyun Lee, Jayesh R. Bhakta, Soonju Choi

QBM

Between at least 1999 and 2005, Kentron Technologies Inc. ("Kentron") invented and developed memory modules based on its Quad Band Memory (*QBM*) technology, well before the July 16, 2009 alleged priority date of the '339 patent. During this time, Kentron formed the QBM Alliance, an alliance of technology partners aimed at positioning QBM as an industry standard. *See*, *e.g.*, SAM-NET00315873. The technical details of the QBM system were regularly disclosed to QBM Alliance members during this time period. *See, e.g.*, SAM-NET00315870-900, SAM-NET00315912. Netlist became a QBM Alliance member in February 2002. *See*, *e.g.*, SAM-NET00315845-47; SAM-NET00315874-81. Because Netlist was a QBM Alliance member, Micron has reason to believe that Netlist knew about the technical features of the QBM system and used the technical features of the QBM system to draft the claims of the '506 patent. The technical features of QBM are shown in the following documents: SAM-NET00314833 - SAM- NET00315913. The invalidity claim chart identifying disclosures from these documents as to the Asserted Claims of the '506 patent is provided in attached Exhibit B20. Kentron did not abandon, suppress, or conceal its invention of QBM. Kentron presented the technical features of QBM to JEDEC, described the features in newsletters to its QBM Alliance members, and filed patents covering the technology. *See, e.g.*, SAM-NET00313593-615, SAM- NET00315870-900, SAM-NET00315171-87, SAM-NET00313434.

JEDEC Proposals

During the time period from at least 2005 to 2012, Netlist regularly attended JEDEC meetings for at least the JC-40 and JC-45 committees, including meetings that occurred before the July 16, 2009 alleged priority date of the '339 patent. *See, e.g.,* SAM-NET00005551-75; SAM-NET00008503-51; SAM-NET00008664-8700; SAM-NET00008847-67; SAM-

NET00019805-18; SAM-NET00020197-98; SAM-NET00023999-24003; SAM-NET00026641-95; SAM-NET00026696-715; SAM-NET00040933-87; SAM-NET00040988-41007; SAM-NET00048535-608; SAM-NET00052084-131; SAM-NET00052132-50; SAM-NET00052917-20; SAM-NET00060465-532; SAM-NET00071314-88; SAM-NET00092148-53; SAM-NET00113524-54; SAM-NET00113555-67.

By virtue of Netlist's attendance at those meetings, active involvement in JEDEC and otherwise, on information and belief, Micron has reason to believe that Netlist was aware of the proposals and drafts being considered and voted upon by those committees. The proposals, drafts, ballots and presentations distributed to the members of the JEDEC committees were distributed to many (20+) key members of the interested public with the expectation they would be freely disclosed to and discussed with others. Based on Netlist's apparent view of the scope of the alleged invention, the proposals, drafts, and presentations disclose materially the same structure and functionality that Netlist accuses of infringing the claims of '339 patent.

After attending these meetings and listening to these ideas from other members of JEDEC, Netlist drafted the application, which Micron has reason to believe contained a significant amount of material Netlist learned at JEDEC.

Lee

Netlist alleges that the '339 patent is entitled to a July 16, 2009 priority date. And yet, three months prior, on April 13, 2009, U.S. Patent No. 8,001,434 to Lee et al. (*Lee*) was filed, disclosing the claimed elements of the '339 patent. While the '339 patent lists Hyun Lee and Jayesh R. Bhakta as inventors, the *Lee* patent lists Hyun Lee, Jayesh R. Bhakta, and Soonju Choi. As such, the inventive entity of the '339 patent differs from the *Lee* patent, therefore the alleged invention of the '339 patent was "made in this country" by "another inventor" under 35

U.S.C. § 102(g)(2). Given that the inventors of *Lee* filed a patent, they did not abandon, suppress, or conceal their invention.

With discovery ongoing, Defendants reserve the right to amend, modify, or supplement these Invalidity Contentions with additional 35 U.S.C. §102(f) and/or (g) allegations should additional information become available through discovery supporting such allegations.

C. U.S. Patent Nos. 11,016,918 and 11,232,054

Invalidity claim charts identifying disclosures in the references identified in Tables 1-C and 2-C as to the Asserted Claims of the '918 and '054 patents are provided in attached Exhibits C1 through C13 ('918 Patent) and Exhibits D1 through D13 ('054 Patent).

Table 1-C: Prior Art Patents and Printed Publications for the '918 and '054 patents

Ex.	Patent No. or Title (Primary Inventor/Author)	Date of Issue/ Publication	Filing Date
RC-1	Asserted Patents Admitted Prior Art (APA)		
RC-2	U.S. Patent Publication No. 2006/0174140 (Harris)	8/3/2006	1/31/2005
RC-3	U.S. Patent Publication No. 2006/0080515 (Spiers)	4/13/2006	10/12/2004
RC-4	U.S. Patent No. 8,189,328 (Kanapathippillai)	5/28/2012	10/22/2007
RC-5	U.S. Patent No. 6,707,724 (Kim)	3/16/2004	2/6/2002
RC-6	JP11-073762 (Okimoto)	3/16/1999	8/28/1997
RC-7	JEDEC Standards	At least as early as June 2000	
RC-8	JP2006-156814 (Ootani)	6/15/2006	11/30/2004
RC-9	Samsung DDR2 Fully Buffered DIMM	11/2006	
RC-10	*A Highly Integrated Power Management IC for Advanced Mobile Applications* (Shi)	09/2006	
RC-11	Maxim MAX1917 Tracking, Sinking and Sourcing, Synchronous Buck Controller for DDR Memory and Termination Supplies (MAX1917)	06/2002	
RC-12	*Central Power Management Unit as Portable Power Management Architecture Based on True Digital*	2004	

Ex.	Patent No. or Title (Primary Inventor/Author)	Date of Issue/ Publication	Filing Date
	Control (Byoun)		
RC-13	JP2002083872A (Ito)	01/29/2004	
RC-14	U.S. Patent No. 7,724,604 (Amidi)	05/25/2010	10/25/2006
RC-15	U.S. Patent No. 6,856,556 (Hajeck)	02/15/2005	04/03/2003
RC-16	U.S. Patent No. 6,670,234 (Hsu)	12/30/2003	06/22/2001
RC-17	U.S. Patent No. 8,316,074 (McManis)	11/20/2012	03/11/2005
RC-20	*The Physical Design of the ILLIAC 6 Supercomputing Platform* (Keller)	2006	
RC-21	SUMMIT Microelectronics Application Note 59, *Platform Solution for DDR SDRAM Power Management* (SUMMIT)	2006	

Table 2-C: Prior Art Systems and Inventions for the '918 and '054 patents

Ex.	Name of System or Invention	Date of Sale / Offer for Sale / Public Use
RC-7	JEDEC Standards	At least as early as June 2000
RC-18	TPS65023	At least as early as June 2006
RC-19	IRU3048	At least as early as September 2002

Defendants have obtained or are in the process of obtaining the identified devices and will make them available for inspection. To the extent that one or more documents (*e.g.*, user manual) may be used to describe aspects of a particular device, that device is a single reference for prior art purposes under 35 U.S.C. § 102. Some or all of the corroborating references may also separately qualify as prior art publications under 35 U.S.C. § 102 and may be used as invalidating references under 35 U.S.C. §§ 102 and/or 103.

Further, Defendants are actively searching for information regarding at least the following devices and inventions:

- JEDEC Standards

- Samsung DDR2 Fully Buffered DIMM
- Infineon Technology Americas Corporation's Rectifier (e.g., IRU3048)
- Micron Technology, Inc.'s DDR2 SDRAM FBDIMM (e.g., MT36HTS51272F, 2006)
- Micron Technology, Inc.'s Elpida 512MB Fully Buffered DIMM (e.g., EBE51FD8AGFD/EBE51FD8AGFN, 2006)
- SK hynix America Inc.'s 240pin Fully Buffered DDR2 SDRAM DIMMs
- Texas Instruments Inc.'s TPS65023

Discovery is ongoing, and Defendants may serve these and other third parties with document subpoenas. One or more of these devices, along with related documentation, may be invalidating, and Defendants reserve the right to supplement these contentions accordingly.

In addition, Defendants identify, responsive to Plaintiff's infringement contentions, the following patents, publications, and systems as examples of evidence of the state of the art as it relates to memory module devices:

- U.S. Patent Publication No. 2006/0174140 (Harris) at [0002] and [0009].
- U.S. Patent Publication No. 2006/0080515 (Spiers) at Fig. 5 and [0037].
- U.S. Patent No. 8,189,328 (Kanapathippillai) at Fig. 1a and 2:55-3:38.
- U.S. Patent No. 6,707,724 (Kim) at Fig 1, Fig. 9, 1:21-45, and 5:56-6:19.
- JP11-073762 (Okimoto) at Fig., 1, [0002], [0021], and [0022].
- JP2006-156814 (Ootani) at Fig. 1, Fig. 9, [0001], [0011], [0021], and [0024].
- Samsung DDR2 Fully Buffered DIMM.
- TPS65023 at page 1.
- IRU3048 at Fig. 2 and page 5.

- Keller at pages 4, 6-7, 11-15, 18, and 23, and at figures 2.1, 2.2, 3.1, 3.2, 3.3, 3.4, 4.1, and 4.2.
- SUMMIT at pages 1-3 and at figures 1-3.

Each of these references show that the concept of incorporating different types of chips into a single module is not novel. Indeed, combining electrical components for enhanced space and data transfer efficiencies and/or power management has been well known for many years. In light of the references discussed herein, the asserted claims of the asserted patents cannot be valid.

Defendants continue to investigate each of the identified devices, including through potential discovery needing to be obtained via third party subpoenas, and reserve the right to supplement these contentions and accompanying claim charts after further investigation.

Defendants' reference to a particular product, device, or software program in these contentions should be interpreted as a reference to the system itself and any corresponding patents, publications, or product literature relating to the cited system. Upon information and belief, the systems were publicly disclosed, used, sold, or offered for sale in the United States before the alleged priority date of the Asserted Claims of the '918 and '054 patents. Defendants' investigation of such prior art systems is still ongoing and discovery has not yet been received from third parties who may have information concerning such prior art systems. Accordingly, subsequent discovery may reveal information that affects the disclosures and contentions herein. For example, subsequent discovery may provide additional information regarding whether or not any of the third party prior art systems anticipate or render obvious the Asserted Claims of the '918 and '054 patents. As such, Defendants reserve all rights to supplement their invalidity contentions.

Many of the inventive, research, design, and development activities concerning these systems and technologies occurred in the United States before the alleged priority date of the Asserted Claims of the '918 and '054 patents. Defendants are in the process of obtaining additional information regarding the dates by which the cited products and services were publicly disclosed, used, sold, or offered for sale, the circumstances under which the research, design, and development activities were conducted, and the identities of the particular individuals involved in such activities through publicly available patents, publications, and product literature. The actual dates, circumstances, and identities of individuals will be the subject of third-party discovery during this lawsuit, which Defendants reserve the right to rely upon to corroborate the prior art status of the prior art identified herein. Defendants reserve the right to modify, amend, or supplement these contentions if additional information becomes available during the course of this lawsuit. Furthermore, Defendants will make all such devices, software programs, or other products in Defendants' possession, custody, or control available for inspection by Plaintiff.

Consequently, Defendants reserve the right to amend, modify, or supplement these Invalidity Contentions should additional information become available to them through discovery. Defendants also reserve the right to assert that the '918 and '054 patents are invalid under 35 U.S.C. §102(f) and/or (g) in the event Defendants obtain evidence that the named inventors of the '918 and '054 patents did not invent (either alone or in conjunction with other parties) the subject matter claimed in the '918 and '054 patents. Should Defendants obtain such evidence, they will provide the name of the person(s) from whom and the circumstances under which the invention or any part of it was derived, and/or the circumstances surrounding the making of the invention before the patent application.

For example, Defendants have reason to believe that individuals substantively involved in the prosecution of the '506 patent knew about material and non-cumulative prior art by virtue of their participation in JEDEC standards meetings. Defendants also assert invalidity of the '918 and '054 patents based on JEDEC documents disclosed and/or publicly available prior to the filing of the '918 and '054 patents. *See* Exhibit C10; *see also* Exhibit D10. With discovery ongoing, Defendants reserve the right to amend, modify, or supplement these Invalidity Contentions with 35 U.S.C. §102(f) and/or (g) allegations should additional information become available through discovery supporting such allegations.

D. U.S. Patent Nos. 8,787,060 and 9,318,160

Invalidity claim charts identifying disclosures in the references identified in Tables 1-D and 2-D as to the Asserted Claims of the '060 and '160 patents are provided in attached Exhibits E1 through E21 ('060 Patent) and Exhibits F1 through F21 ('160 Patent).

Table 1-D: Prior Art Patents and Printed Publications for the '060 and '160 patents

Ex.	Patent No. or Title (Primary Inventor/Author)	Date of Issue/ Publication	Filing Date
RD-1	Asserted Patents Admitted Prior Art (APA)		
RD-2	U.S. Patent Application Publication No. 2008/0025137 (Rajan 137)	1/31/2008	7/31/2006
RD-3	U.S. Patent Application Publication No. 2011/0103156 (Kim)	5/5/2011	12/29/2009
RD-4	U.S. Patent No. 9,142,262 (Ware)	4/28/2011	9/24/2010
RD-5	U.S. Patent Application Publication No. 2011/0026293 (Riho 293)	2/3/2011	7/16/2010
RD-6	U.S. Patent Application Publication No. 2010/0195364 (Riho 364)	8/5/2010	2/1/2010
RD-7	U.S. Patent Application Publication No. 2010/0091537 (Best)	4/15/2010	12/13/2007
RD-8	U.S. Patent No. 8,258,619 (Foster)	5/12/2011	11/12/2009
RD-9	U.S. Patent Application Publication No.	5/6/2010	10/30/2008

Ex.	Patent No. or Title (Primary Inventor/Author)	Date of Issue/ Publication	Filing Date
	2010/0110745 (Jeddeloh)[6]		
RD-10	U.S. Patent Application Publication No. 2011/0208906 (Gillingham)	8/25/2011	12/14/2010
RD-11	U.S. Patent No. 8,120,958 (Bilger)	6/25/2009	12/24/2007
RD-12	U.S. Patent No. 9,123,552 (Keeth)	10/6/2011	3/30/2010
RD-13	U.S. Patent No. 7,969,192 (Wyman)	7/15/2010	3/26/2010
RD-14	U.S. Patent No. 9,160,349 (Ma)	3/3/2011	8/27/2009
RD-15	U.S. Patent No. 7,796,446 (Ruckerbauer)	3/25/2010	9/19/2008
RD-16	Gabriel H. Loh, 3D-Stacked Memory Architectures for Multi-Core Processors, Georgia Institute of Technology, International Symposium on Computer Architecture (2008) (Loh)	June 2008	
RD-17	U.S. Patent No. 8,041,881 (Rajan 881)	10/18/2011	6/12/2007

Table 2-D: Prior Art Systems and Inventions for the '060 and '160 patents

Ex.	Name of System or Invention	Date of Sale / Offer for Sale / Public Use
RD-18	JEDEC Proposals regarding High Bandwidth Memory (HBM) and Low Power Memories (JEDEC HBM and Low Power Proposals)	At least as early as September 2009, December 2009, March 2010, June 2010, September 2010, April 2011, June 2011, September 2011
RD-19	Micron Hybrid Memory Cube	At least as early as August 2010
RD-20	U.S. Patent No. 8,471,362 (Lee)	At least as early as April 5, 2011
RD-21	Micron LRDIMM System	At least as early as 2010

Defendants have obtained or are in the process of obtaining the identified devices and will make them available for inspection. To the extent that one or more documents (*e.g.*, user manual) may be used to describe aspects of a particular device, that device is a single reference for prior art purposes under 35 U.S.C. § 102. Some or all of the corroborating references may also

[6] *See also*, for further background and explanation, U.S. Patent No. 7,623,365 also to Joe M. Jeddeloh ("Jeddeloh 365"), which was filed on August 29, 2007, and issued on November 24, 2009.

separately qualify as prior art publications under 35 U.S.C. § 102 and may be used as invalidating references under 35 U.S.C. §§ 102 and/or 103.

Micron Hybrid Memory Cube System ("Micron HMC System") was offered for sale or publicly used or the information known at least as early as August 2010. Micron employees gave presentations about the Micron HMC Systems at conferences (e.g., Hot Chips) and to other companies, including one or more employees of IBM, Cisco, Juniper, and Sony during the relevant time frame. Micron also filed a patent relating to the research involved with the Micron HMC System, referenced herein as Keeth (RD-12).

Micron LRDIMM System was offered for sale or publicly used or the information known at least as early as 2010. Various Micron LRDIMM Systems were publicly sold on variety of websites and Micron even made at least one data sheet available for public dissemination during the relevant time frame.

Discovery is ongoing, and Defendants may serve other third parties with document subpoenas. One or more of these devices, along with related documentation, may be invalidating, and Defendants reserve the right to supplement these contentions accordingly.

In addition, Defendants identify, responsive to Plaintiff's infringement contentions, the following patents, publications, and systems as examples of evidence of the state of the art as it relates to memory module devices:

Ex.	Patent No. or Title (Primary Inventor/Author)
RD-1	Asserted Patents Admitted Prior Art (APA)
RD-2	U.S. Patent Application Publication No. 2008/0025137 (Rajan 137)
RD-3	U.S. Patent Application Publication No. 2011/0103156 (Kim)
RD-4	U.S. Patent No. 9,142,262 (Ware)
RD-5	U.S. Patent Application Publication No. 2011/0026293 (Riho 293)
RD-6	U.S. Patent Application Publication No. 2010/0195364 (Riho 364)

Ex.	Patent No. or Title (Primary Inventor/Author)
RD-7	U.S. Patent Application Publication No. 2010/0091537 (Best)
RD-8	U.S. Patent No. 8,258,619 (Foster)
RD-9	U.S. Patent Application Publ. No. 2010/0110745 (Jeddeloh); *see also* Jeddeloh 365
RD-10	U.S. Patent Application Publication No. 2011/0208906 (Gillingham)
RD-11	U.S. Patent No. 8,120,958 (Bilger)
RD-12	U.S. Patent No. 9,123,552 (Keeth)
RD-13	U.S. Patent No. 7,969,192 (Wyman)
RD-14	U.S. Patent No. 9,160,349 (Ma)
RD-15	U.S. Patent No. 7,796,446 (Ruckerbauer)
RD-16	Gabriel H. Loh, *3D-Stacked Memory Architectures for Multi-Core Processors, Georgia Institute of Technology, International Symposium on Computer Architecture* (2008) (Loh)
RD-17	U.S. Patent No. 8,041,881 (Rajan 881)
RD-18	JEDEC Proposals regarding High Bandwidth Memory (HBM) and Low Power Memories (JEDEC HBM and Low Power Proposals)
RD-19	Micron Hybrid Memory Cube
RD-20	U.S. Patent No. 8,471,362 (Lee)
RD-21	Micron LRDIMM System

Each of these references show that the concept of reducing the load of drivers in a memory package on a memory module is not novel. Indeed, reducing the load of drivers on the memory module for enhanced data transfer efficiencies and/or power management has been well known for many years. In light of the references discussed herein, the Asserted Claims of the '060 and '160 patents cannot be valid.

Defendants continue to investigate each of the identified devices, including through potential discovery needing to be obtained via third party subpoenas, or from Plaintiff, and reserve the right to supplement these contentions and accompanying claim charts after further investigation.

Defendants' reference to a particular product, device, or software program in these

contentions should be interpreted as a reference to the system itself and any corresponding patents, publications, or product literature relating to the cited system. Upon information and belief, the systems were publicly disclosed, used, sold, or offered for sale in the United States before the alleged priority date of the Asserted Claims of the '060 and '160 patents. Defendants' investigation of such prior art systems is still ongoing and discovery has not yet been received from third parties who may have information concerning such prior art systems. Accordingly, subsequent discovery may reveal information that affects the disclosures and contentions herein. For example, subsequent discovery may provide additional information regarding whether or not any of the third party prior art systems anticipate or render obvious the Asserted Claims of the '060 and '160 patents. As such, Defendants reserve all rights to supplement their invalidity contentions.

Many of the inventive, research, design, and development activities concerning these systems and technologies occurred in the United States before the alleged priority date of the Asserted Claims of the '060 and '160 patents. Defendants are in the process of obtaining additional information regarding the dates by which the cited products and services were publicly disclosed, used, sold, or offered for sale, the circumstances under which the research, design, and development activities were conducted, and the identities of the particular individuals involved in such activities through publicly available patents, publications, and product literature. The actual dates, circumstances, and identities of individuals will be the subject of third party discovery during this lawsuit, which Defendants reserve the right to rely upon to corroborate the prior art status of the prior art identified herein. Defendants reserve the right to modify, amend, or supplement these contentions if additional information becomes available during the course of this lawsuit. Furthermore, Defendants will make all such devices, software programs, or other

products in Defendants' possession, custody, or control available for inspection by Plaintiff. Consequently, Defendants reserve the right to amend, modify, or supplement these Invalidity Contentions should additional information become available to them through discovery.

Table 4-D provides additional bases for invalidity of the '060 and '160 patents under pre-AIA 35 U.S.C. § 102(f), on the grounds that the inventors of the '060 and '160 patents did not themselves invent the subject matter claimed in the '060 patent. The prior art under § 102(f) is identified in Table 4-D by the name of the person(s) from whom the invention was derived. The circumstances under which the invention was derived are explained below.

Table 4-D: Prior Art under pre-AIA § 102(f) for the '060 and '160 patents

Ex.	Prior Art Disclosing Technical Features	Name of Person(s) from Whom Invention was Derived
RD-18	Proposals and disclosures made at JEDEC committee meetings during the time period 2009-2011 ("*JEDEC HBM and Low Power Proposals*")	Entities and persons attending JEDEC committee meetings where related technology was discussed (including the JC-42 committee meetings). For example: • One or more employees of ST Ericsson • One or more employees of the Industrial Technology Research Institute • One or more employees of Hynix • One or more employees of Elpida • One or more employees of Intel • One or more employees of Nokia • One or more employees of Samsung • One or more employees of LSI • One or more employees of AMD • One or more employees of Advantest • One or more employees of Avago Technologies • One or more employees of Samsung • One or more employees of Fusion • One or more employees of NVIDIA • One or more employees of Nanya

Hyun Lee – an inventor of the '060 and '160 patents – regularly attended JEDEC meetings for at least the JC-42 committee in the 2009 to 2011 timeframe, as well as before and after that timeframe

By virtue of his attendance at those meetings, active involvement in JEDEC and otherwise, Micron has reason to believe that Hyun Lee was aware of the proposals and draft and final specifications for memory packages being considered and voted upon by those committees. Micron has reason to believe: for example, ST Ericsson presented and discussed Committee Item Number 1776.10 ("MIPI M-PHY Future Mobile PHY Proposal") at the September 2009 meeting of JC-42; Samsung presented and discussed Committee Item Number 1777.00 ("Wide-IO TG Report") at the December 2009 meeting of JC- 42; the Industrial Technology Research Institute presented and discussed Committee Item Number 1782.01 ("Advanced Memory Package Proposal") at the March 2010 meeting of JC-42; and NVIDIA presented and discussed Committee Item Number 1797.00 ("Future High Bandwidth Memory TG") at the September 2011 meeting of JC-42, all of which Hyun Lee attended.

Draft specifications, ballots and presentations distributed to the members of the JC-42 committee of JEDEC were distributed to many (20+) key members of the interested public with the expectation they would be freely disclosed to and discussed with others. Based on Netlist's apparent view of the scope of the alleged invention, each of the memory package-related drafts and presentations disclose materially the same structure and functionality that Netlist accuses of infringing the claims of '060 and '160 patents.

Before November 3, 2010, after attending the above-referenced meetings and observing those ideas from other members of JEDEC, Micron has reason to believe that Hyun Lee returned to Netlist and drafted the provisional application to which the '060 and '160 patents claim

priority, deriving the alleged inventions of the '060 and '160 patents from what he learned at JEDEC. He filed the provisional on November 3, 2010, naming himself as the inventor. On November 3, 2011, Hyun Lee filed the application leading to the '060 patent, which Micron has reason to believe contained a significant amount of new material learned at JEDEC and again named himself as inventor.

Table 5-D below provides additional bases for invalidity of the '060 and '160 patent under pre-AIA 35 U.S.C. § 102(g)(2), on the grounds that the alleged invention of the '060 patent was made in this country before the alleged invention date of the '060 patent by another inventor who had not abandoned, suppressed, or concealed it. The prior art under § 102(g)(2) is identified in Table 5-D by the name of the person(s) or entities involved in the making of the invention before the applicants of the '060 patent. The circumstances surrounding the making of the invention before the applicants of the '060 patent are explained below.

Table 5-D: Prior Art under pre-AIA § 102(g)(2) for the '060 and '160 patents

Ex.	Prior Art Disclosing Technical Features	Name of Person(s)
RD-18	Proposals and disclosures made at JEDEC committee meetings during the time period 2009-2011 ("*JEDEC HBM and Low Power Proposals*")	Entities and persons attending JEDEC committee meetings where related technology was discussed (including the JC-42 committee meetings). For example: • One or more employees of ST Ericsson • One or more employees of the Industrial Technology Research Institute • One or more employees of Hynix • One or more employees of Elpida • One or more employees of Intel • One or more employees of Nokia • One or more employees of Samsung • One or more employees of LSI • One or more employees of AMD

Ex.	Prior Art Disclosing Technical Features	Name of Person(s)
		• One or more employees of Advantest • One or more employees of Avago Technologies • One or more employees of Samsung • One or more employees of Fusion • One or more employees of NVIDIA • One or more employees of Nanya
RD-19	Micron Hybrid Memory Cube	One or more employees of Micron. Circumstances of development discussed above regarding public availability.

Hyun Lee – an inventor of the '060 and '160 patents – regularly attended JEDEC meetings for at least the JC-42 committee in the 2009 to 2011 timeframe, as well as before and after that timeframe

By virtue of his attendance at those meetings, active involvement in JEDEC and otherwise, Micron has reason to believe that Hyun Lee was aware of the proposals and draft and final specifications for memory packages being considered and voted upon by those committees. Micron has reason to believe: for example, ST Ericsson presented and discussed Committee Item Number 1776.10 ("MIPI M-PHY Future Mobile PHY Proposal") at the September 2009 meeting of JC-42; Samsung presented and discussed Committee Item Number 1777.00 ("Wide-IO TG Report") at the December 2009 meeting of JC- 42; the Industrial Technology Research Institute presented and discussed Committee Item Number 1782.01 ("Advanced Memory Package Proposal") at the March 2010 meeting of JC-42; and NVIDIA presented and discussed Committee Item Number 1797.00 ("Future High Bandwidth Memory TG") at the September 2011 meeting of JC-42, all of which Hyun Lee attended.

Draft specifications, ballots and presentations distributed to the members of the JC-42 committee of JEDEC were distributed to many (20+) key members of the interested public with

the expectation they would be freely disclosed to and discussed with others. Based on Netlist's apparent view of the scope of the alleged invention, each of the memory package-related drafts and presentations disclose materially the same structure and functionality that Netlist accuses of infringing the claims of '060 and '160 patents.

Before November 3, 2010, after attending the above-referenced meetings and observing those ideas from other members of JEDEC, Micron has reason to believe that Hyun Lee returned to Netlist and drafted the provisional application to which the '060 and '160 patents claim priority, and which Micron has reason to believe contained a significant amount of material Hyun Lee and Netlist learned at JEDEC. He filed the provisional on November 3, 2010, naming himself as the inventor. On November 3, 2011, Hyun Lee filed the application leading to the '060 patent, which Micron has reason to believe contained a significant amount of new material learned at JEDEC and again named himself as inventor.

With discovery ongoing, Defendants reserve the right to amend, modify, or supplement these Invalidity Contentions with 35 U.S.C. § 102(f) and/or (g) allegations should additional information become available through discovery supporting such allegations.

IV. P.R. 3-3(b) – Invalidity Grounds

Pursuant to P.R. 3-3(b), Defendants contend that certain prior art references below anticipate one or more Asserted Claims and that to the extent the identified prior art references do not anticipate the Asserted Claims, those claims are invalid as obvious under 35 U.S.C. §103. Each anticipatory prior art reference, either alone or in combination with other prior art, also renders the Asserted Claims invalid as obvious. In particular, each anticipatory prior art reference may be combined with (1) information generally known to persons skilled in the art at the time of the alleged invention, and/or (2) any of the other anticipatory prior art references. To the extent that Plaintiff contends that any of the anticipatory prior art fails to disclose one or

Defendants' search for prior art references, additional documentation, and/or corroborating evidence concerning prior art systems and devices is ongoing. Accordingly, Defendants reserve the right to supplement their production as Defendants obtain additional prior art references, documentation, and/or corroborating evidence concerning invalidity during the course of discovery.

Dated: November 21, 2022

Respectfully submitted,

By: */s/ Michael R. Rueckheim*

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CERTIFICATE OF SERVICE

I hereby certify that, on November 21, 2022, a copy of the foregoing and Exhibits A-F attached thereto were served to all counsel of record.

By: */s/ Michael R. Rueckheim*
Michael R. Rueckheim